

FIG. 1

```

$ date
    2/28/2004 1:30:15 PM
$end

$version
    Example Clean Receive Data
$end

$timescale
    1ps
$end

$scope module U $end
$var wire 1 !!RxD ReceiveData $end
$upscope $end

$enddefinitions $end

#0
$dumpvars
1!!RxD
$end
#70
0!!RxD
#120
1!!RxD
#170
0!!RxD
#220
1!!RxD
#270
0!!RxD

```

**FIG. 2A**

```

$ date
    2/28/2004 1:30:15 PM
$end

$version
    Example Clean Receive
Data
$end

$timescale
    1ps
$end

$scope module U $end
$var wire 1 !!RxD ReceiveData
$end
$upscope $end

$enddefinitions $end

#0
$dumpvars
1!!RxD
$end
#75
0!!RxD
#125
1!!RxD
#165
0!!RxD
#230
1!!RxD
#265
0!!RxD

```

**FIG. 3A**

```

$date
    2/28/2004 1:30:15 PM
$end

$version
    Example Clean Receive Data
$end

$timescale
    1ps
$end

$scope module U $end
$var wire 1 !!RxD ReceiveData $end
$upscope $end

$enddefinitions $end

#0
$dumpvars
1!!RxD
$end
#75
0!!RxD
#130
1!!RxD
#185
0!!RxD
#240
1!!RxD
#295
0!!RxD

```

**FIG. 4A**

```

$date
    2/28/2004 1:30:15 PM
$end

$version
    Example Clean Receive Data
$end

$timescale
    1ps
$end

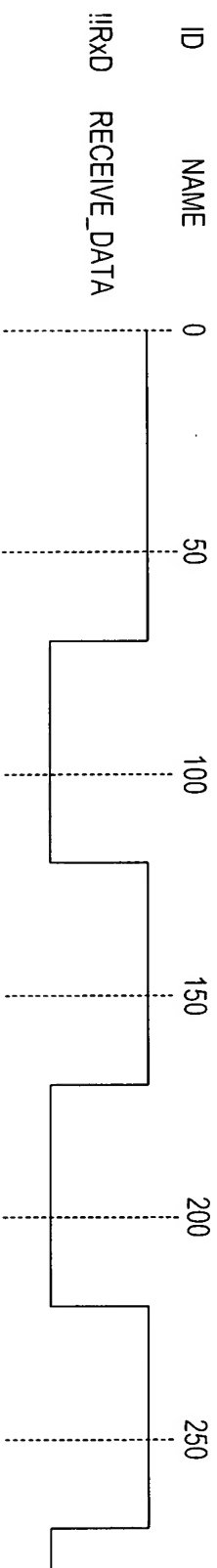
$scope module U $end
$var wire 1 !!RxD ReceiveData $end
$upscope $end

$enddefinitions $end

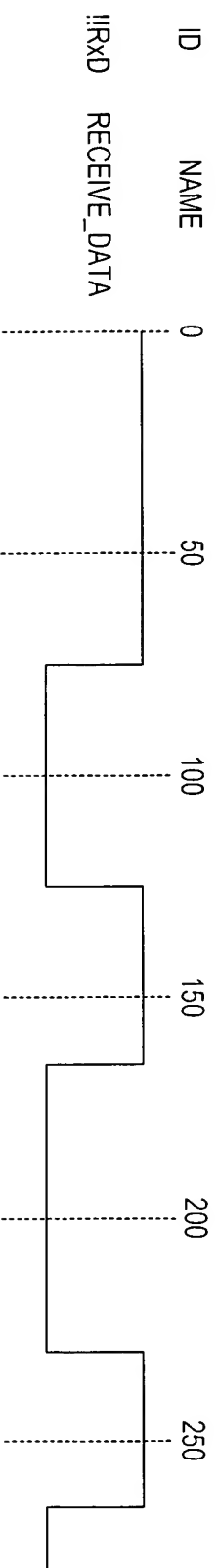
#0
$dumpvars
1!!RxD
$end
#80
0!!RxD
#135
1!!RxD
#180
0!!RxD
#250
1!!RxD
#290
0!!RxD

```

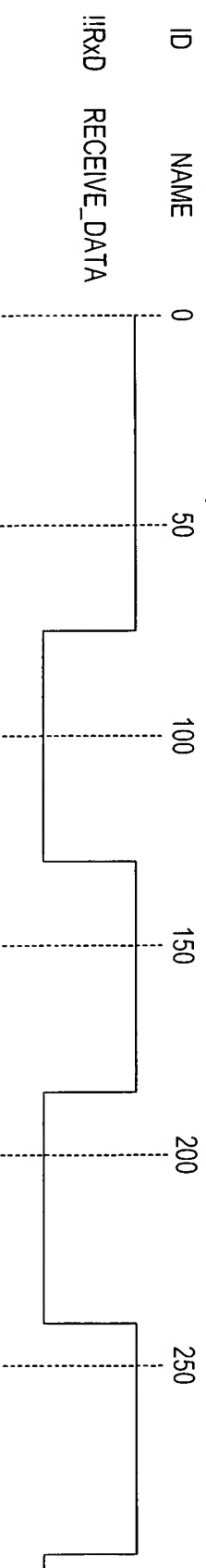
**FIG. 5A**



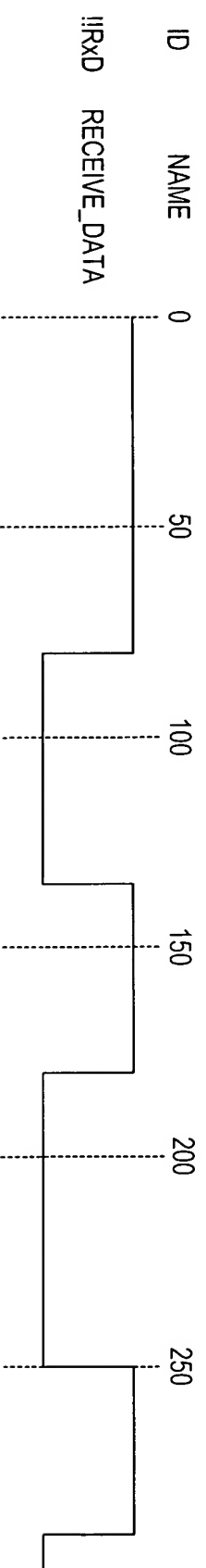
**FIG. 2B**



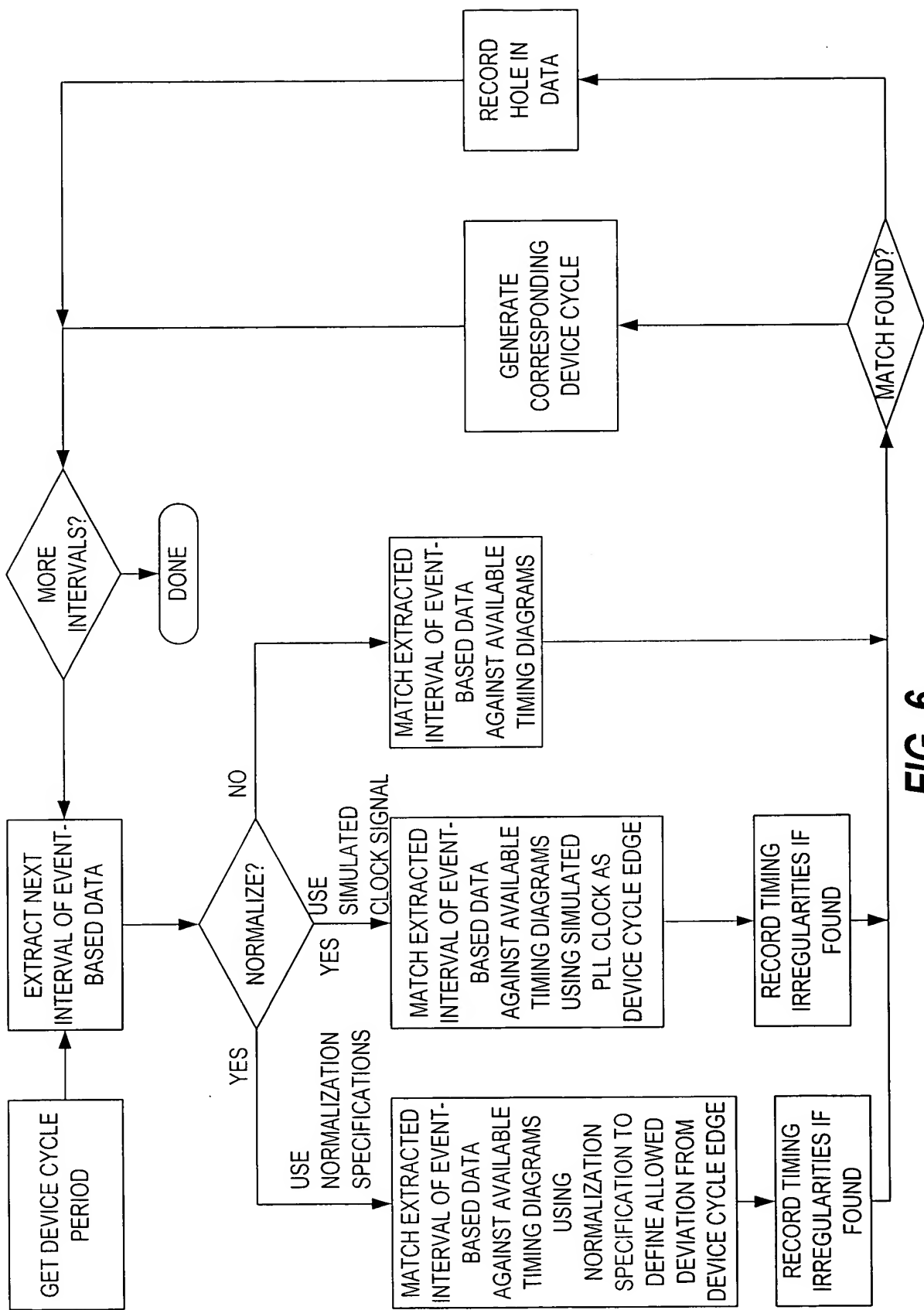
**FIG. 3B**



**FIG. 4B**

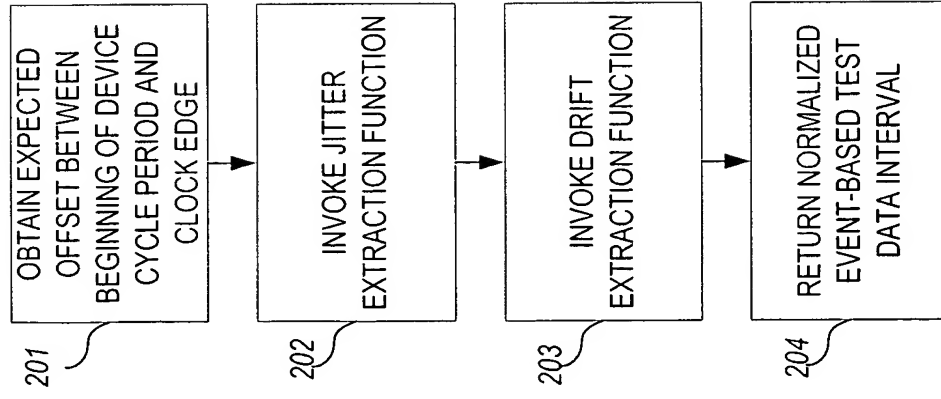


**FIG. 5B**



**FIG. 6**

200



**FIG. 7**

210

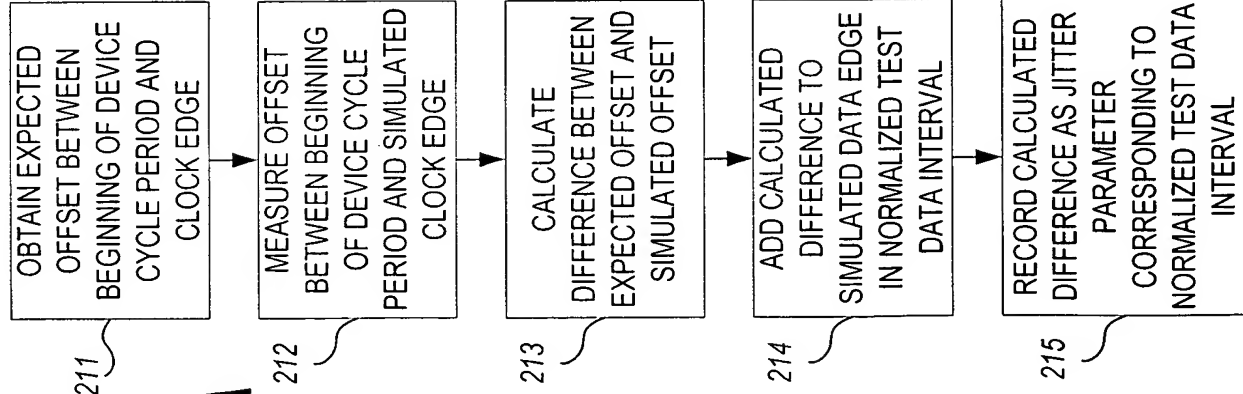


FIG. 8A

220

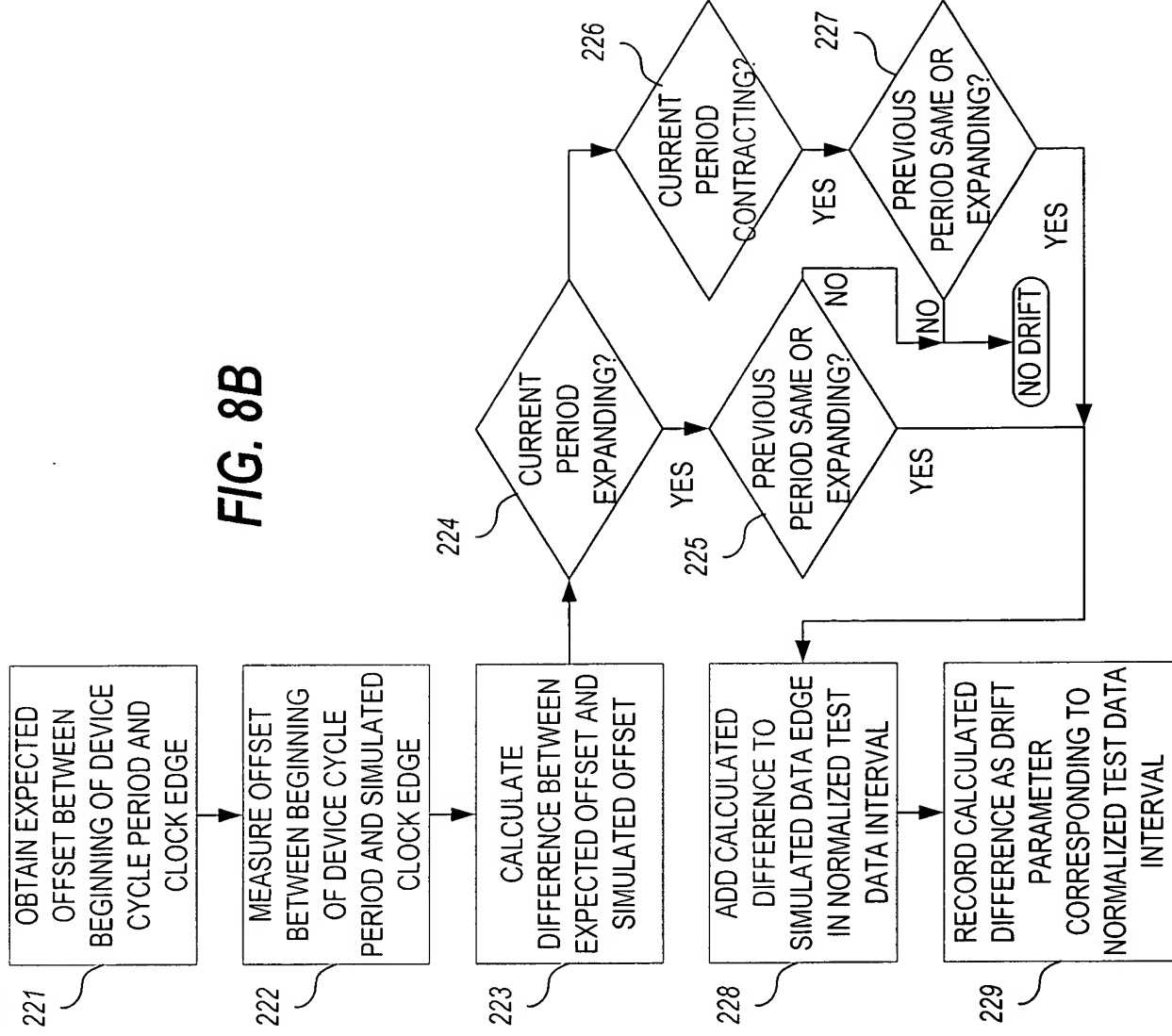


FIG. 8B

```

$ date
2/28/2004 1:30:15 PM
$end

$version
Jitter Example
$end

$timescale
1ps
$end

$scope module U $end
$var wire 1 !!
$var wire 1 !!RxD ReceiveData
$end
$var wire 1 !!RxCLK ReceiveClock
$end
$upscope $end

$enddefinitions $end

#0
$dumpvars
0!!RxCLK
1!!RxD
$end
#55
1!!RxCLK
#75
0!!RxD
#105
0!!RxCLK
#125
1!!RxD
#145
1!!RxCLK
#165
0!!RxD
#210
0!!RxCLK
#230
1!!RxD
#245
1!!RxCLK
#265
0!!RxD

```

**FIG. 9A**

```

$ date
2/28/2004 1:30:15 PM
$end

$version
Drift Example
$end

$timescale
1ps
$end

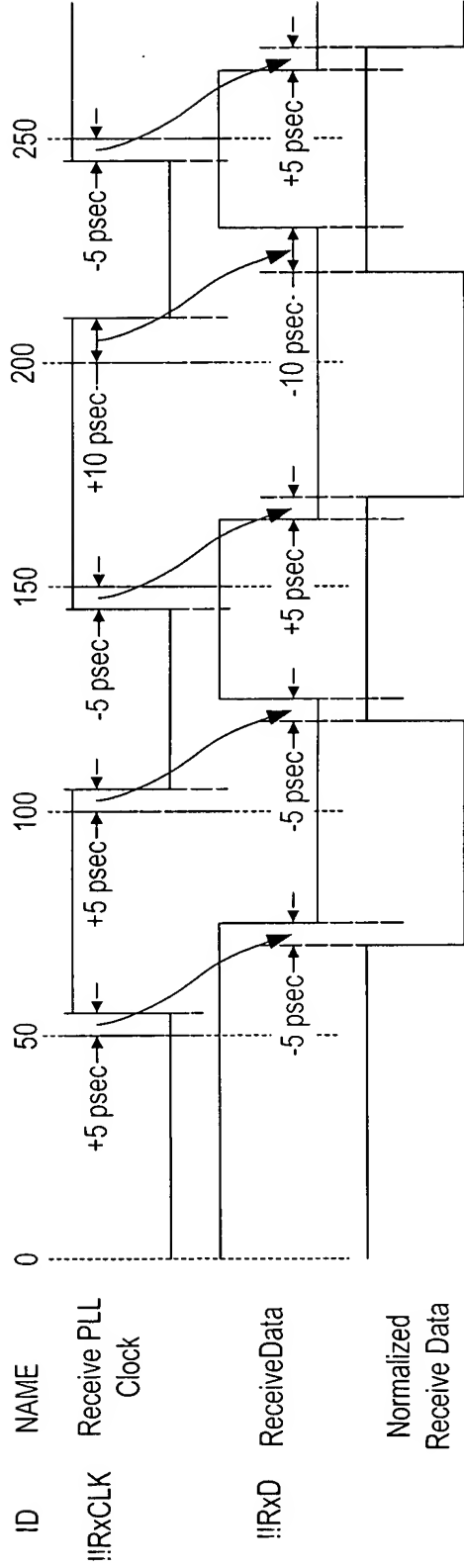
$scope module U $end
$var wire 1 !!
$var wire 1 !!RxD ReceiveData
$end
$var wire 1 !!RxCLK ReceiveClock
$end
$upscope $end

$enddefinitions $end

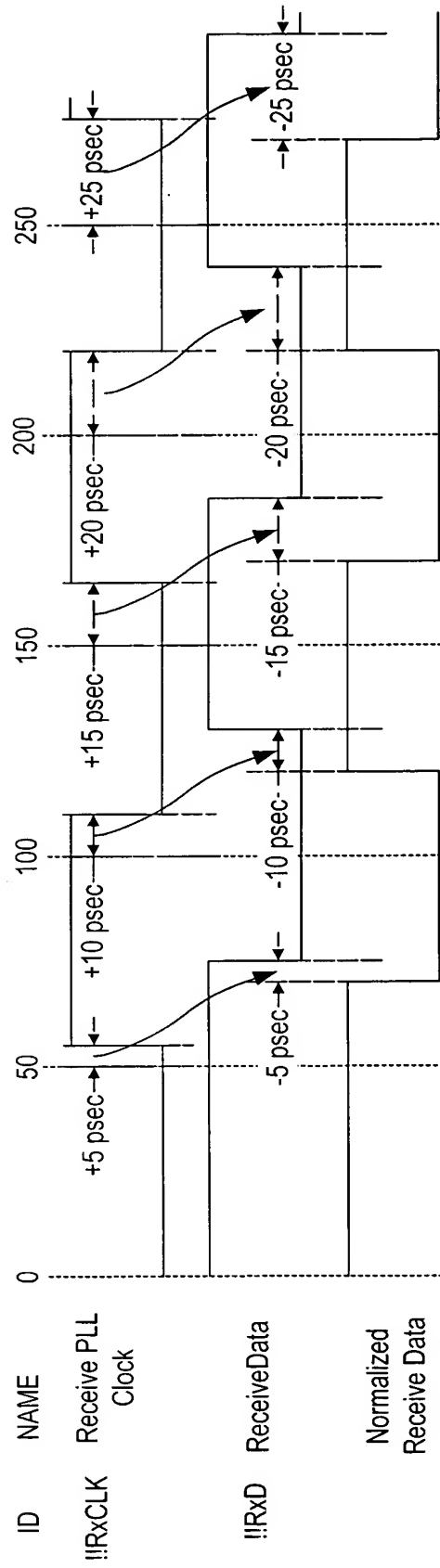
#0
$dumpvars
0!!RxCLK
1!!RxD
$end
#55
1!!RxCLK
#75
0!!RxD
#110
0!!RxCLK
#125
1!!RxD
#165
1!!RxCLK
#165
0!!RxD
#220
0!!RxCLK
#230
1!!RxD
#275
1!!RxCLK
#265
0!!RxD

```

**FIG. 10A**



**FIG. 9B**



**FIG. 10B**

230

240

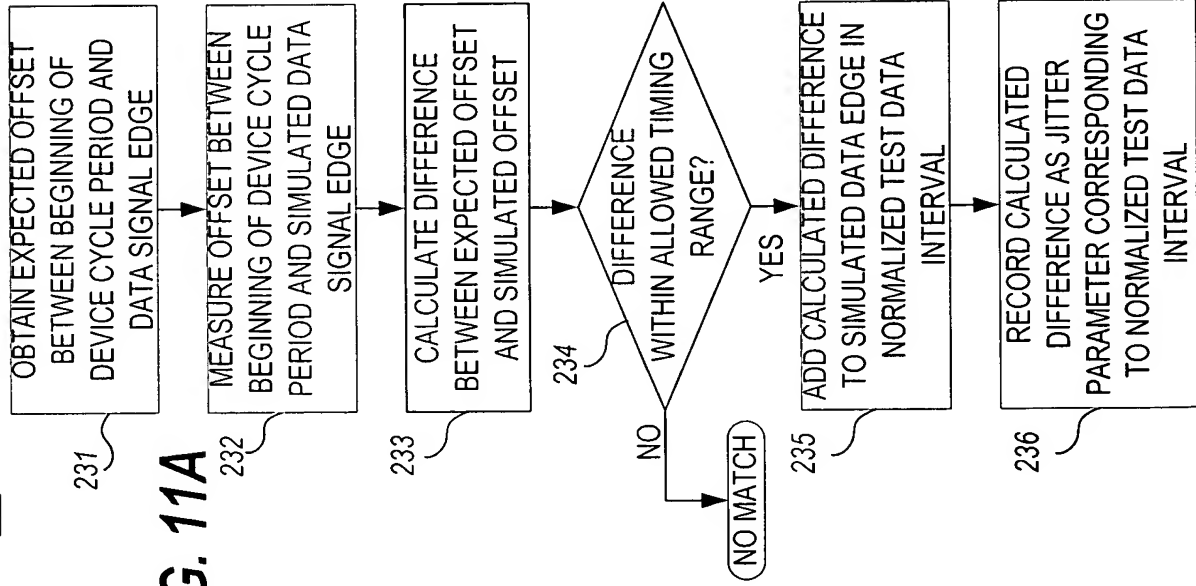


FIG. 11A

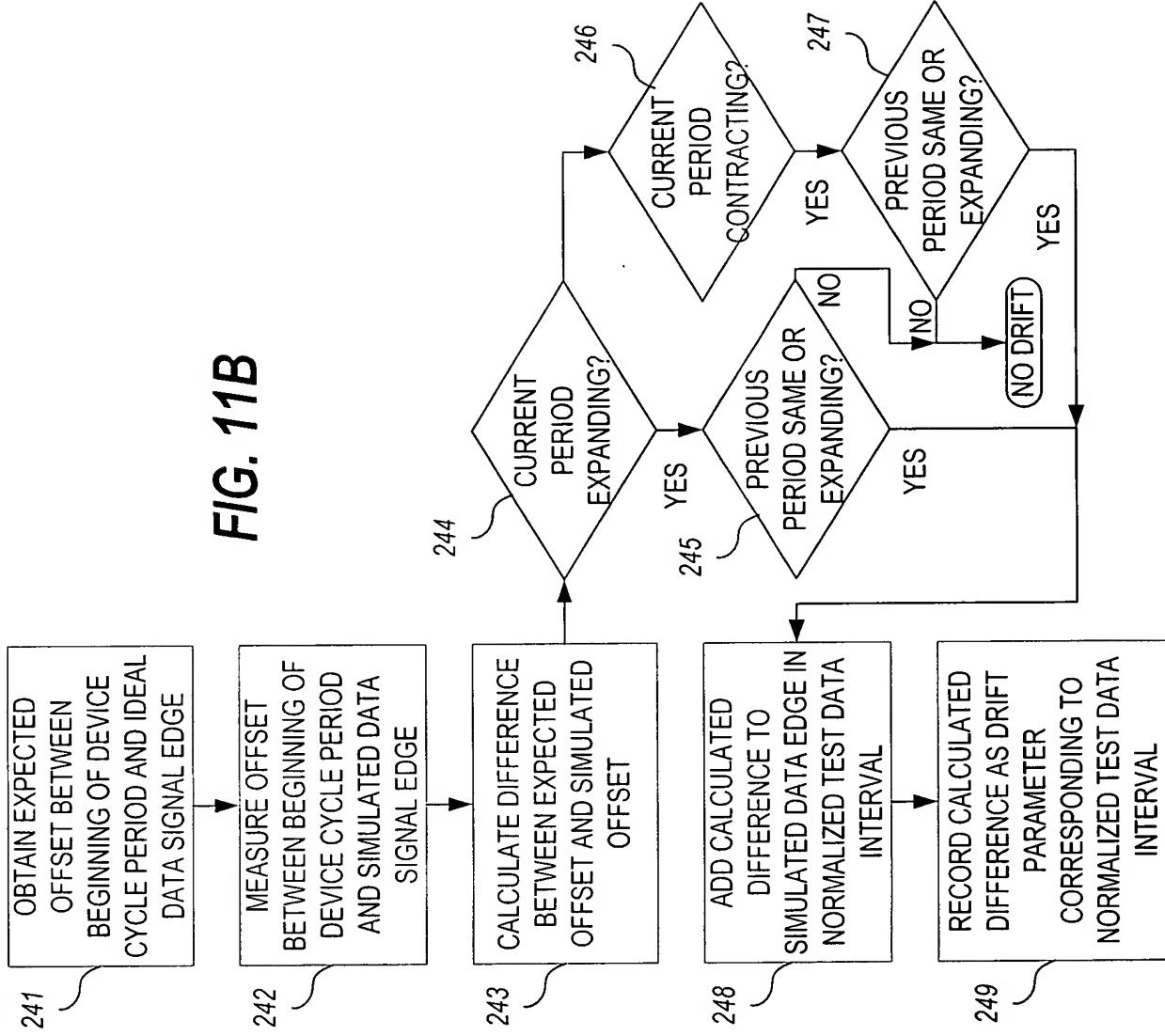


FIG. 11B